超大型積體電路設計導論　Homework Assignment #5

Due date: 109/12/31

[8.3] Consider the logic chain shown in Figure P8.1. The input at A is switched from a 1 to a 0. Find an expression for the delay time through the chain using the procedure developed for the network shown in Figure 8.6.

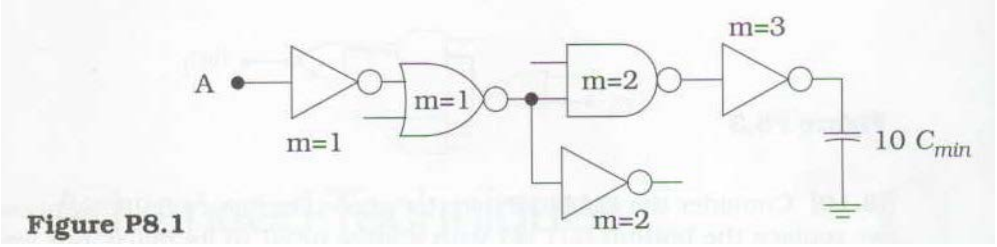


Figure P8.1

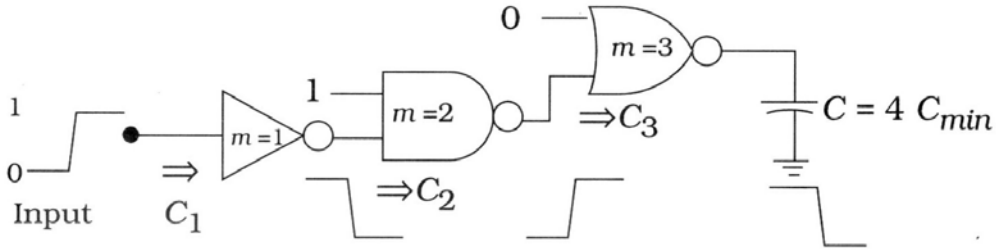


Figure 8.6

[8.6] An interconnect line is described by a capacitance per unit length of c' = 0.86 pF/cm. The line itself runs over a significant portion of the chip and has a total length of 272 μm. A "standard" inverter has an input capacitance of 52 fF and uses symmetrical devices with $\beta_n = \beta_p$. The mobility ratio is r = 2.8 for the process. This is used as the first stage in a driver chain for the interconnect.

Use the idealized theory to design the driver chain with the constraint that the output must be non-inverting.

[8.8] Consider the logic cascade shown in Figure P8.2. Use Logical Effort to find the relative size of each stage needed to minimize delay through the chain. Assume symmetric gates with r = 2.5.

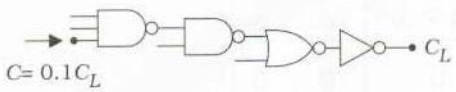


Figure P8.2

[8.9] The logic chain in Figure P8.3 is constructed in a process with r = 2.5. Determine the optimum sizing for each stage for the "highlighted" path indicated using the technique of Logical Effort.

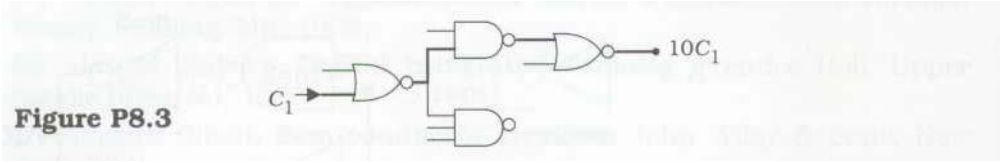


Figure P8.3

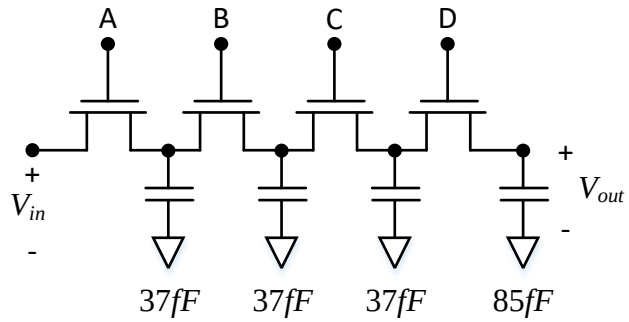
9.8 Design a clocked CMOS circuit that implements the function $f = \overline{a \cdot (b + c) + x \cdot y}$

9.11 Draw the circuit diagram for a dynamic logic gate that has an output of $f = \overline{a \cdot b + c \cdot a}$ using the smallest number of transistors

9.14 Four nFETs are used as pass transistor as shown below, the input voltage is set to $V_{in}=V_{DD}=5V$, and it is given that $V_{Tn}=0.75V$.

a) for the first case, suppose that the signals are initially at (A,B,C,D)=(1,1,0,0) and are then switched to (A,B,C,D)=(0,0,1,1). Find the final value of V_{out}

b) suppose instead that sigals are initially at (A,B,C,D)=(1,1,1,0) and are then switched to (A,B,C,D)=(0,0,1,1). Find the final value of V_{out}



9.16 Find the CVSL gate for the function table shown below by constructing an nFET logic tree

f	1	1	0	1	0	0	1	1
c	0	1	0	1	0	1	0	1
b	0	0	1	1	0	0	1	1
a	0	0	0	0	1	1	1	1