Introduction to VLSI Design, 2020 Fall

Homework assignment #1 Due date: 2020/10/8

Chapter 2 problems

[2.3] The output of an nFET is used to drive the gate of another nFET as shown in Figure P2.3. Assume that $V_{DD} = 3.3$ V and $V_{Tn} = 0.60$ V. Find the output voltage V_{out} when the input voltages are at the following values: (a) $V_a = 3.3$ V and $V_b = 3.3$ V; (b) $V_a = 0.5$ V and $V_b = 3.0$ V; (c) $V_a = 2.0$ V and $V_b = 2.5$ V; (d) $V_a = 3.3$ V and $V_b = 1.8$ V.

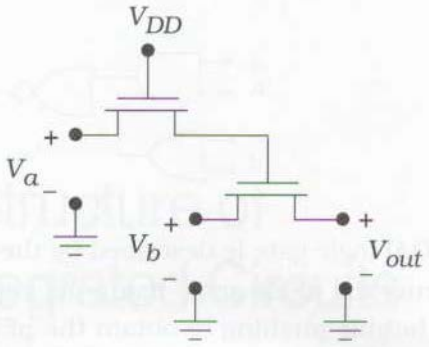


Figure P2.3

[2.6] Consider the 2-input XOR function $a \oplus b$.

(a) Design an XOR gate using a 4:1 MUX.

(b) Modify the circuit in (a) to produce a 2-input XNOR.

(c) A full adder accepts inputs a, b, and c and calculates the sum bit

$$s = a \oplus b \oplus c \tag{2.85}$$

Use your MUX-based gates to design a circuit with this output.

[2.8] Design a CMOS circuit for the OAI expression

$$h = \overline{(a+b)\cdot(a+c)\cdot(b+d)} \tag{2.87}$$

Use the smallest number of transistors in your design.

[2.12] An AOAI logic gate is described by the schematic in Figure P2.5.

(a) Construct the nFET array using the logic diagram.

(b) Apply bubble pushing to obtain the pFET logic. Use the diagram to construct the pFET array using the pFET rules.

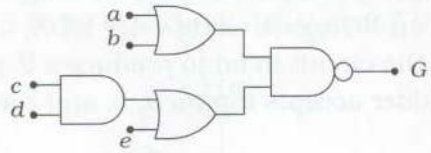


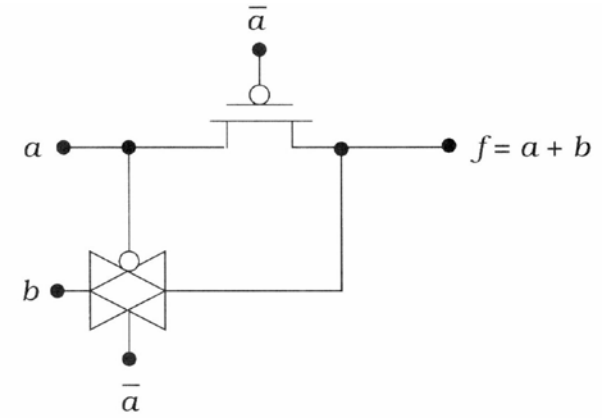
Figure P2.5

[2.14] Design the 4:1 multiplexor circuit that implements the function in equation (2.80) by using TG switches.

$$F = P_0 \cdot \overline{S}_1 \cdot \overline{S}_0 + P_1 \cdot \overline{S}_1 \cdot S_0 + P_2 \cdot S_1 \cdot \overline{S}_0 + P_3 \cdot S_1 \cdot S_0 \quad (2.80)$$

[2.15]

Convert the following design to an AND gate



[2.16] For the following truth table, please use

(a) AOI logic

(b) OAI logic

to implement the design (draw the CMOS schematic). Use the true but not the complementary forms of A,B,C only as input

AB \ C	0	1
00	1	1
01	1	0
11	0	0
10	1	0

[2.17] For the following MOS circuit

a) What is the Boolean function of Y?

b) Assume node X is the input of the inverter, what are the maximum and minimum voltages of X

c) draw the equivalent design using fully complementary CMOS logic, assume complementary forms of input signals are available